

# Add RVV support for V8

## RoadMap:

### Phase I: Prepare

1. Investigate the RVV extension encode
  - Investigate how to add rvv for assembler
  - Investigate how to add rvv for disassembler
2. Investigate code gen of TurboFan and liftoff, Vector register allocation
3. Investigate how to simulate RVV instruction. We can refer to spike.

### Phase II: Implement rvv

There are two strategies:

- Imitate and copy mips64 simd api and arch opcode. Implement macro assembler api by rvv.

Simply and implement quickly but maintenance may be difficult.

- Implement simd arch opcode and code-gen independently.

Harder to achieve